Input low voltage
Input high voltage
Output low voltage
Output high voltage
Clock input low voltage
Clock input high voltage
Clock output low voltag
Clock output high volta
Input leakage
Clock input leakage
Silence voltage
Peak to peak speech o
External load on speec

30	ZERO
31	A
32	B
33	C
34	D
35	E
36	F
37	G
38	H
39	I
40	J
41	K
42	L
43	M
44	N

t_{WSS}
I_F
t_{SU}
t_W
t_H

Table 3 **A.C. switch**

ROMS

Paramet
Chip select access t
Output turn off dela
Address access tim
Input capacitance C
Output capacitance

sequence

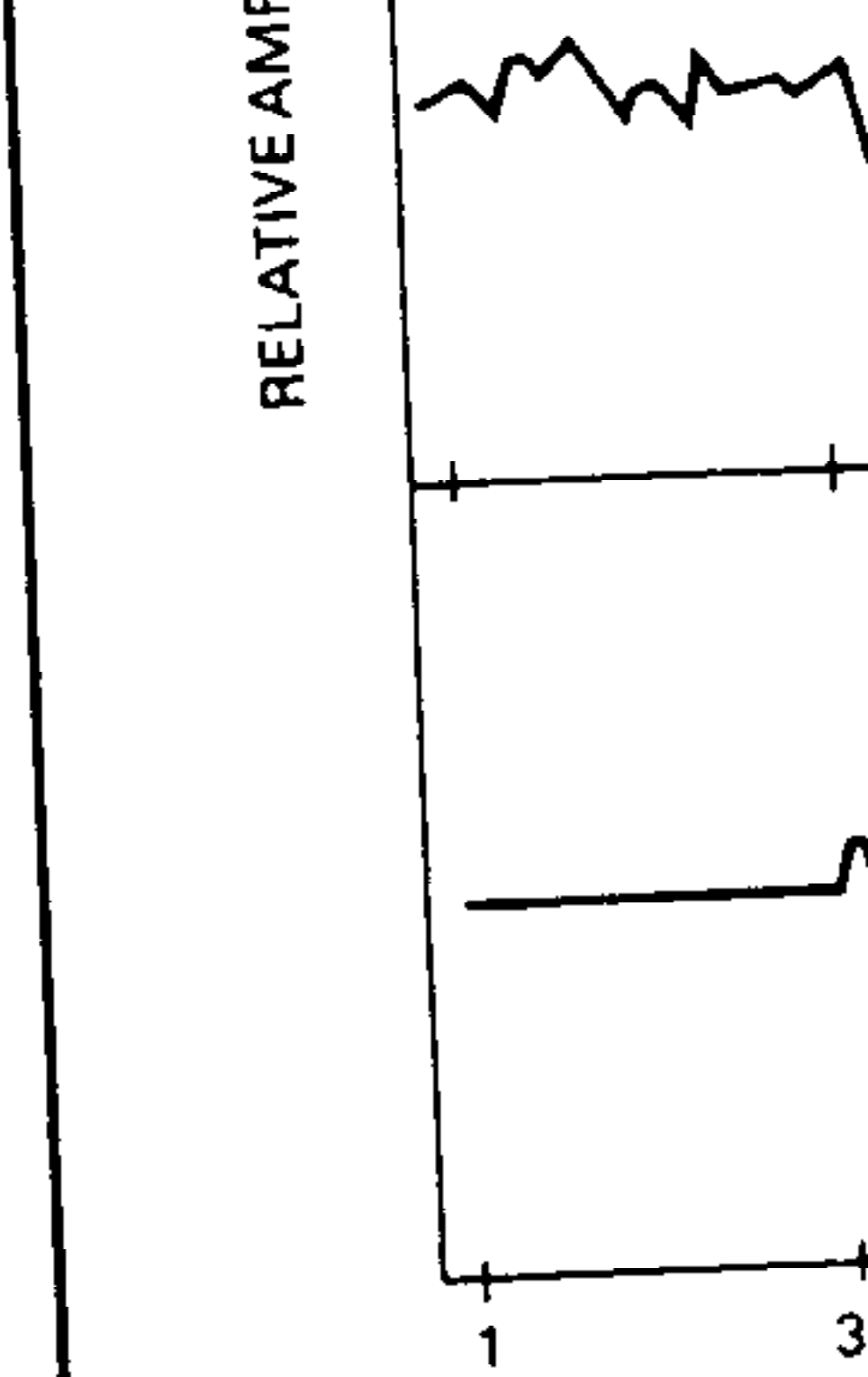
1 Reset interrupt

$\overline{WR}$ Write strobe

The write strobe line latche
(SW1-SW8) into an internal
edge of $\overline{WR}$ the speech pro
of the command specified b
sequence is shown in the t
1. If a command to start a n
issued during a speech seq
will be started immediately
to a switch it must be a si
type.

R data 1-8 ROM data

This is the 8-bit parallel data
speech data from the speech



(a) Original Spee
(b) Phase Angle
(c) Half-Period Z

IO_{15}

A high on SW4 line during
the audio output to be muted

Figure 5 **ROM Select seque**

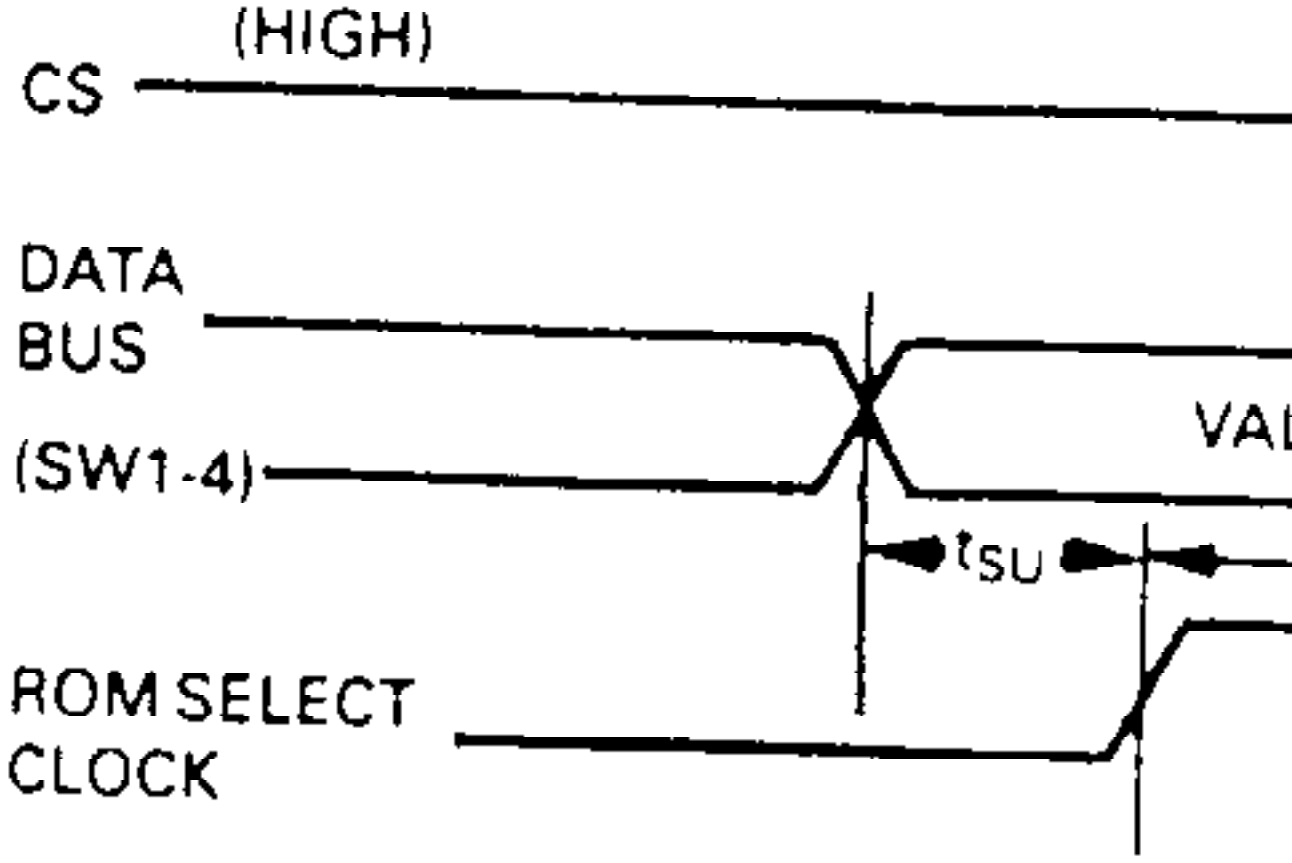


Figure 6 **Speech synthesis circui**