National Semiconductor

# DS78LS120/DS88LS120 Dual Differential Line Receiver (Noise Filtering and Fail-Safe)

## General Description

The DS78LS120 and DS88LS120 are high performance, dual differential, TTL compatible line receivers for both balanced and unbalanced digital data transmission. The inputs are compatible with EIA, Federal and MIL standards.

The line receiver will discriminate a ±200 mV input signal over a common-mode range of ±10V and a ±300 mV signal over a range of ±15V.

Circuit features include hysteresis and response control for applications where controlled rise and fall times and/or high frequency noise rejection are desirable. Threshold offset control is provided for fail-safe detection, should the input be open or short. Each receiver includes an optional 180Ω terminating resistor and the output gate contains a logic strobe for time discrimination. The DS78LS120 is specified over a −55°C to +125°C temperature range and the DS88LS120 from 0°C to +70°C.

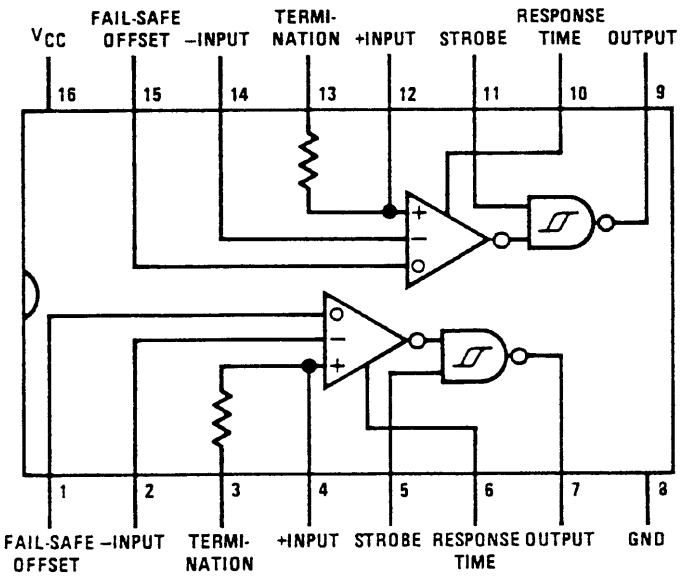
Input specifications meet or exceed those of the popular DS7820/DS8820 line receiver.

## Features

- Meets EIA standards RS232-C, RS422 and RS423, Federal Standards 1020, 1030 and MIL-188-114
- Input voltage range of ±15V (differential or common-mode)
- Separate strobe input for each receiver
- 5k typical input impedance
- Optional 180Ω termination resistor
- 50 mV input hysteresis
- 200 mV input threshold
- Separate fail-safe mode

## Connection Diagram

**Dual-In-Line Package**

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**Top View**

**Order Number DS88LS120N or DS88LS120M**
**See NS Package Number M16A or N16A**

**For Complete Military 883 Specifications, see RETS Data Sheet.**
**Order Number DS78LS120J/883 or DS78LS120W/883**
**See NS Package Number J16A or W16A**

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | ±25V |
| Strobe Voltage | 7V |
| Output Sink Current | 50 mA |
| Storage Temperature Range | −65°C to +150°C |
| Maximum Power Dissipation* at 25°C | |
| Cavity Package | 1433 mV |
| Molded Package | 1362 mW |
| Lead Temperature (Soldering, 4 sec) | 260°C |

*Derate cavity package 9.6 mW/°C above 25°C; derate molded package 10.9 mW/°C above 25°C.

## Operating Conditions

| | Min | Max | Units |
|---|---|---|---|
| Supply Voltage ($V_{CC}$) | 4.5 | 5.5 | V |
| Temperature ($T_A$) | | | |
| DS78LS120 | −55 | +125 | °C |
| DS88LS120 | 0 | +70 | °C |
| Common-Mode Voltage ($V_{CM}$) | −15 | +15 | V |

## Electrical Characteristics (Notes 2 and 3)

| Symbol | Parameter | Conditions | | Min | Typ | Max | Ur |
|---|---|---|---|---|---|---|---|
| $V_{TH}$ | Differential Threshold Voltage | $I_{OUT}$ = −400 μA, $V_{OUT}$ ≥ 2.5V | −7V ≤ $V_{CM}$ ≤ 7V | | 0.06 | 0.2 | V |
| | | | −15 ≤ $V_{CM}$ ≤15V | | 0.06 | 0.3 | V |
| $V_{TL}$ | Differential Threshold Voltage | $I_{OUT}$ = 4 mA, $V_{OUT}$ ≤ 0.5V | −7V ≤ $V_{CM}$ ≤7V | | −0.08 | −0.2 | V |
| | | | −15V ≤ $V_{CM}$ ≤ 15V | | −0.08 | −0.3 | V |
| $V_{TH}$ $V_{TL}$ | Differential Threshold Voltage with Fail-Safe Offset = 5V | $I_{OUT}$ = −400 μA, $V_{OUT}$ ≥ 2.5V | −7V ≤ $V_{CM}$ ≤ 7V | | 0.47 | 0.7 | |
| | | $I_{OUT}$ = 4 mA, $V_{OUT}$ ≤ 0.5V | −7V ≤ $V_{CM}$ ≤ 7V | −0.2 | −0.42 | | |
| $R_{IN}$ | Input Resistance | −15V ≤ $V_{CM}$ ≤ 15V, 0V ≤ $V_{CC}$ ≤ 7V | | 4 | 5 | | k |
| $R_T$ | Line Termination Resistance | $T_A$ = 25°C | | 100 | 180 | 300 | Ω |
| $R_O$ | Offset Control Resistance | $T_A$ = 25°C | | 42 | 56 | 70 | k |
| $I_{IND}$ | Data Input Current (Unterminated) | $V_{CM}$ = 10V | 0V ≤ $V_{CC}$ ≤ 7V | | 2 | 3.1 | m |
| | | $V_{CM}$ = 0V | | | 0 | −0.5 | m |
| | | $V_{CM}$ = −10V | | | −2 | −3.1 | m |
| $V_{THB}$ | Input Balance (Note 5) | $I_{OUT}$ = −400 μA, $V_{OUT}$ ≥ 2.5V, $R_S$ = 500Ω | −7V ≤ $V_{CM}$ 7V | | 0.1 | 0.4 | |
| | | $I_{OUT}$ = 4 mA, $V_{OUT}$ ≤ 0.5V, $R_S$ = 500Ω | −7V ≤ $V_{CM}$ ≤ 7V | | −0.1 | −0.4 | |
| $V_{OH}$ | Logical "1" Output Voltage | $I_{OUT}$ = −400 μA, $V_{DIFF}$ = 1V, $V_{CC}$ = 4.5V | | 2.5 | 3 | | |
| $V_{OL}$ | Logical "0" Output Voltage | $I_{OUT}$ = 4 mA, $V_{DIFF}$ = −1V, $V_{CC}$ = 4.5V | | | 0.35 | 0.5 | |
| $I_{CC}$ | Power Supply Current | $V_{CC}$ = 5.5V, $V_{DIFF}$ = −0.5V, (Both Receivers) | $V_{CM}$ = 15V | | 10 | 16 | m |
| | | | $V_{CM}$ = −15V | | 10 | 16 | m |
| $I_{IN\ (1)}$ | Logical "1" Strobe Input Current | $V_{STROBE}$ = 5.5V, $V_{DIFF}$ = 3V | | | 1 | 100 | μ |
| $I_{IN\ (0)}$ | Logical "0" Strobe Input Current | $V_{STROBE}$ = 0V, $V_{DIFF}$ = −3V | | | −290 | −400 | μ |
| $V_{IH}$ | Logical "1" Strobe Input Voltage | $V_{OL}$ ≤ 0.5, $I_{OUT}$ = 4mA | | 2.0 | 1.12 | | |
| $V_{IL}$ | Logical "0" Strobe Input Voltage | $V_{OH}$ ≥ 2.5V, $I_{OUT}$, = −400 μA | | | 1.12 | 0.8 | |
| $I_{OS}$ | Output Short-Circuit Current | $V_{OUT}$ = 0V, $V_{CC}$ = 5.5V, $V_{STROBE}$ = 0V, (Note 4) | | −30 | −100 | −170 | m |

**Note 1:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual devic operation.

**Note 2:** Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS78LS120 and across the 0°C to +70°C for th DS88LS120. All typical values are for $T_A$ = 25°C, $V_{CC}$ = 5V and $V_{CM}$ = 0V.

**Note 3:** All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values show as max or min on absolute value basis.

**Note 4:** Only one output at a time should be shorted.

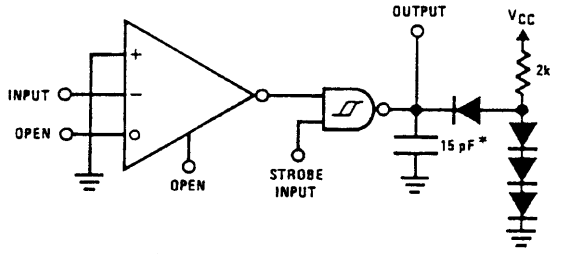
**Note 5:** Refer to EIA-RS422 for exact conditions.

## Switching Characteristics $V_{CC}$ = 5V, $T_A$ = 25°C

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{pd0(D)}$ | Differential Input to "0" Output | Response Pin Open, $C_L$ = 15 pF, $R_L$ = 2 kΩ | | 38 | 60 | ns |
| $t_{pd1(D)}$ | Differential Input to "1" Output | | | 38 | 60 | ns |
| $t_{pd0(S)}$ | Strobe Input to "0" Output | | | 16 | 25 | ns |
| $t_{pd1(S)}$ | Strobe Input to "1" Output | | | 12 | 25 | ns |

## AC Test Circuit and Switching Time Waveforms

**Differential and Strobe Input Signal**

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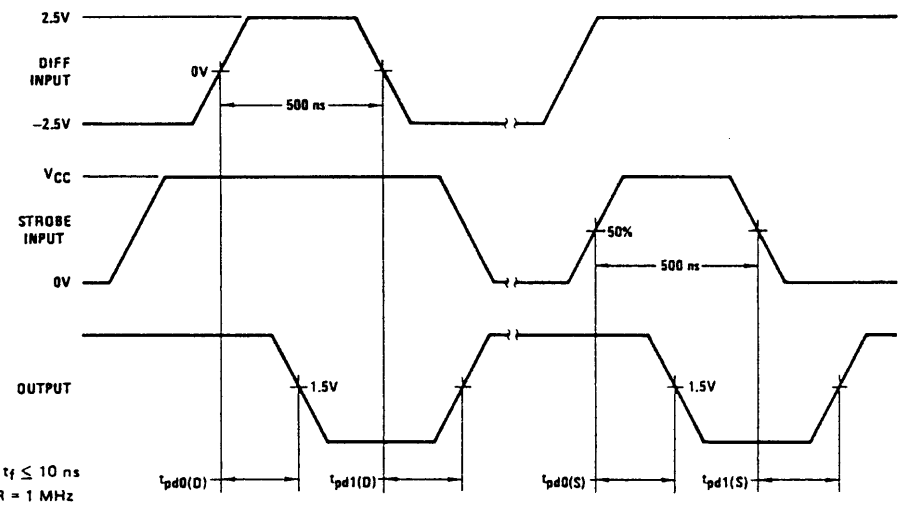
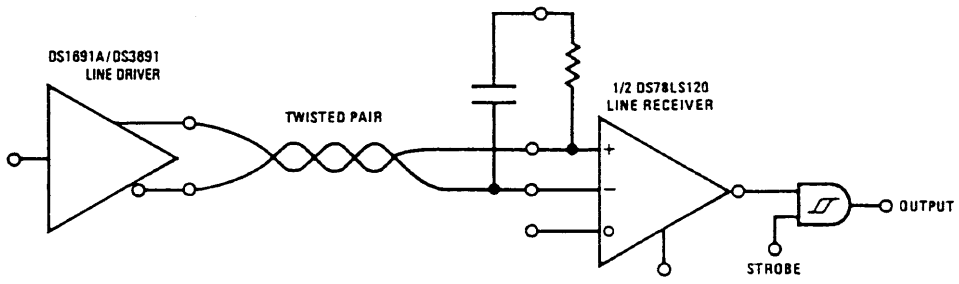
*Includes probe and test fixture capacitance




**Note:** Optimum switching response is obtained by minimizing stray capacitance on Response Control pin (no external connection). TL/F/7499–4

## Application Hints

**Balanced Data Transmission**

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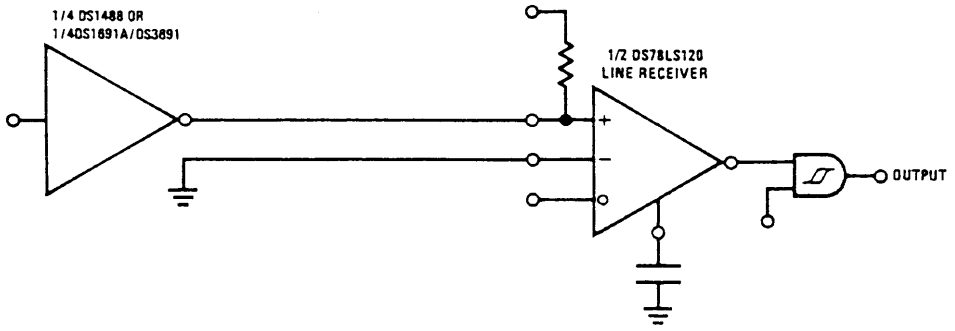
## Application Hints (Continued)

### Unbalanced Data Transmission

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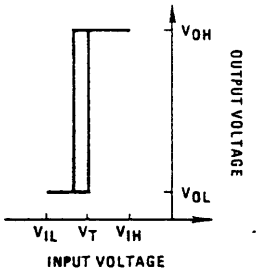
### Logic Level Translator

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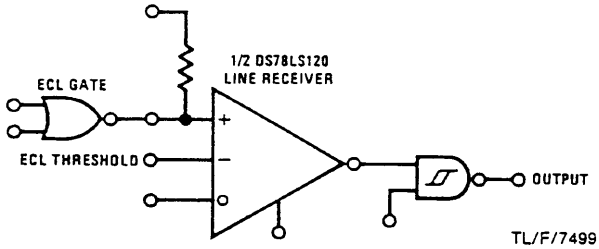


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The DS78LS120/DS88LS120 may be used as a level translator to interface between ±12V MOS, ECL, TTL and CMOS. To configure, bias either input to a voltage equal to ½ the voltage of the input signal, and the other input to the driving gate.

### LINE DRIVERS

Line drivers which will interface with the DS78LS120/DS88LS120 are listed below.

**Balanced Drivers**

| | |
|---|---|
| DS26LS31 | Quad RS-422 Line Driver Dual CMOS |
| DS7830, DS8830 | Dual TTL |
| DS7831, DS8831 | Dual TRI-STATE TTL |
| DS7832, DS8832 | Dual TRI-STATE TTL |
| DS1691A, DS3691 | Quad RS-423/Dual RS-422 TTL |
| DS1692, DS3692 | Quad RS-423/Dual TRI-STATE RS-422 TTL |
| DS3487 | Quad TRI-STATE RS-422 |

**Unbalanced Drivers**

| | |
|---|---|
| DS1488 | Quad RS-232 |
| DS75150 | Dual RS-232 |

### RESPONSE CONTROL AND HYSTERESIS

In unbalanced (RS-232/RS-423) applications it is recommended that the rise time and fall time of the line driver be controlled to reduce cross-talk. Elimination of switching noise is accomplished in the DS78LS120/DS88LS120 by the 50 mV of hysteresis incorporated in the output gate. This eliminates the oscillations which may appear in a line receiver due to the input signal slowly varying about the threshold level for extended periods of time.

High frequency noise which is superimposed on the input signal which may exceed 50 mV can be reduced in amplitude by filtering the device input. On the DS78LS120/DS88LS120, a high impedance response control pin in the input amplifier is available to filter the input signal without affecting the termination impedance of the transmissic line. Noise pulse width rejection vs the value of the r sponse control capacitor is shown in *Figures 1* and *2*. Th combination of filters followed by hysteresis will optimi: performance in a worse case noise environment.

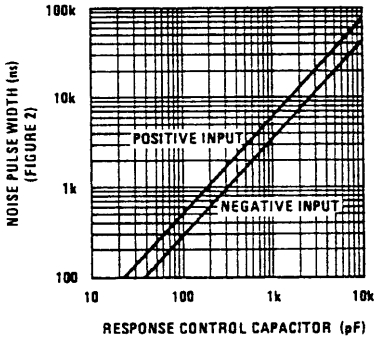


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**FIGURE 1. Noise Pulse Width vs Response Control Capacitor**

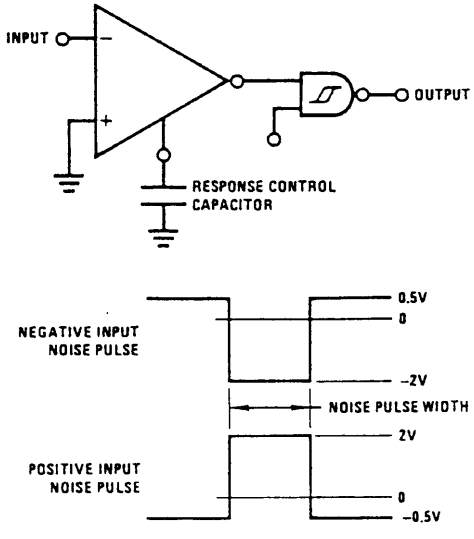


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**FIGURE 2**

## Application Hints (Continued)

### TRANSMISSION LINE TERMINATION

On a transmission line which is electrically long, it is advisable to terminate the line in its characteristic impedance to prevent signal reflection and its associated noise/crosstalk. A 180Ω termination resistor is provided in the DS78LS120/DS88LS120 line receiver. To use the termination resistor, connect pins 2 and 3 together and pins 13 and 14 together. The 180Ω resistor provides a good compromise between line reflections, power dissipation in the driver, and IR drop in the transmission line. If power dissipation and IR drop are still a concern, a capacitor may be connected in series with the resistor to minimize power loss.

The value of the capacitor is recommended to be the line length (time) divided by 3 times the resistor value. Example: if the transmission line is 1,000 feet long, (approximately 1000 ns), and the termination resistor value is 180Ω, the capacitor value should be 1852 pF. For additional application details, refer to application notes AN-22 and AN-108.

### FAIL-SAFE OPERATION

Communication systems require elements of a system to detect the presence of signals in the transmission lines, and it is desirable to have the system shut-down in a fail-safe mode if the transmission line is open or shorted. To facilitate the detection of input opens or shorts, the DS78LS120/DS88LS120 incorporates an input threshold voltage offset. This feature will force the line receiver to a specific logic state if presence of either fault is a condition.

Given that the receiver input threshold is ±200 mV, an input signal greater than ±200 mV insures the receiver will be in a specific logic state. When the offset control input (pins 1 and 15) is connected to $V_{CC}$ = 5V, the input thresholds are offset from 200 mV to 700 mV, referred to the non-inverting input, or −200 mV to −700 mV, referred to the inverting input. Therefore, if the input is open or shorted, the input will be greater than the input threshold and the receiver will remain in a specified logic state.

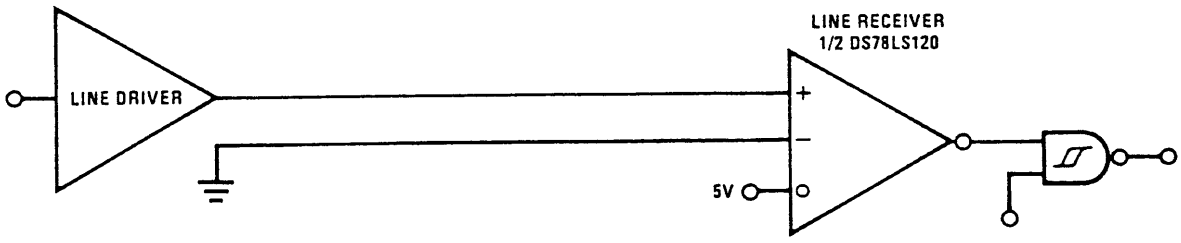
The input circuit of the receiver consists of a 5k resistor terminated to ground through 120Ω on both inputs. This network acts as an attenuator, and permits operation with common-mode input voltages greater than ±15V. The offset control input is actually another input to the attenuator, but its resistor value is 56k. The offset control input is connected to the inverting input side of the attenuator, and the input voltage to the amplifier is the sum of the inverting input plus 0.09 times the voltage on the offset control input. When the offset control input is connected to 5V the input amplifier will see $V_{IN(INVERTING)}$ +0.45V or $V_{IN(INVERTING)}$ +0.9V when the control input is connected to 10V. The offset control input will not significantly affect the differential performance of the receiver over its common-mode operating range, and will not change the input impedance balance of the receiver.

It is recommended that the receiver be terminated (500Ω or less) to insure it will detect an open circuit in the presence of noise.

The offset control can be used to insure fail-safe operation for unbalanced interface (RS-423) or for balanced interface (RS-422) operation.

For unbalanced operation, the receiver would be in an indeterminate logic state if the offset control input was open. Connecting the fail-safe offset pin to 5V, offsets the receiver threshold to 0.45V. The output is forced to a logic zero state if the input is open or shorted.

**Unbalanced RS-423 and RS-232 Fail-Safe**

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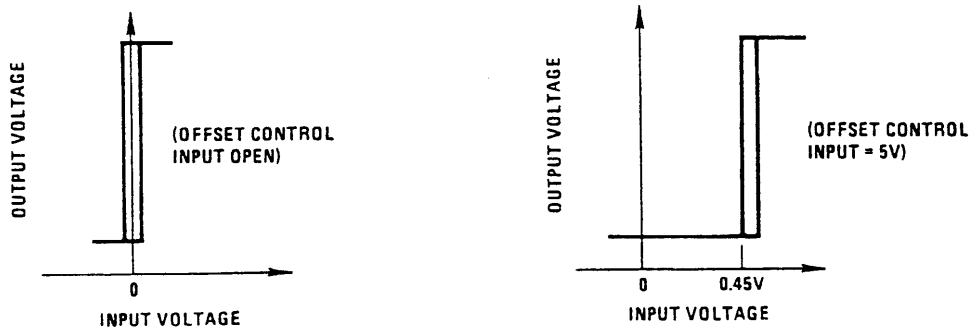


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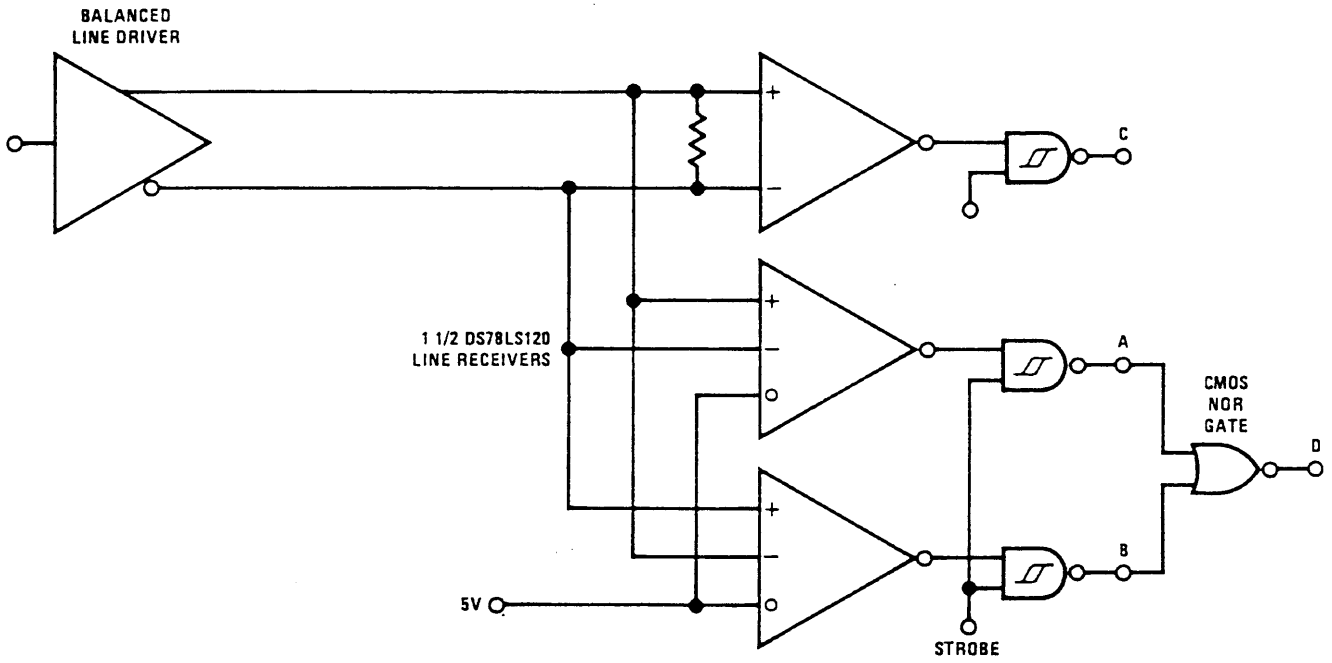
## Application Hints (Continued)

**Balanced RS-422 Fail-Safe**

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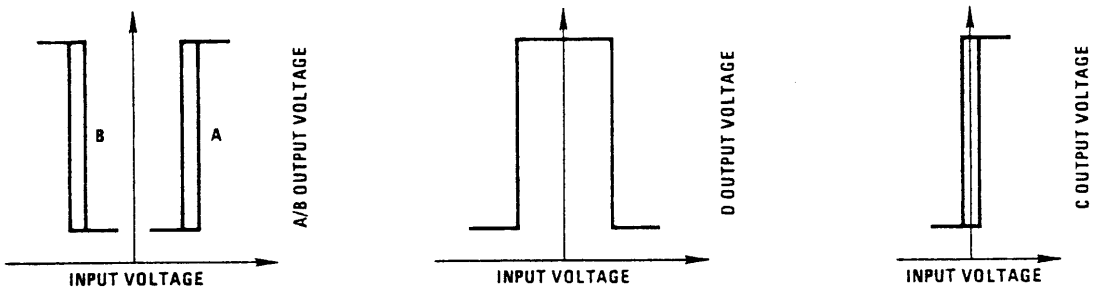


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For balanced operation with inputs open or shorted, receiver C will be in an indeterminate logic state. Receivers A and B will be in a logic zero state allowing the NOR gate to detect the open or short condition. The strobe will disable receivers A and B and may therefore be used to sample the fail-safe detector. Another method of fail-safe detection consists of filtering the output of NOR gate D so it would not indicate a fault condition when receiver inputs pass through the threshold region, generating an output transient.

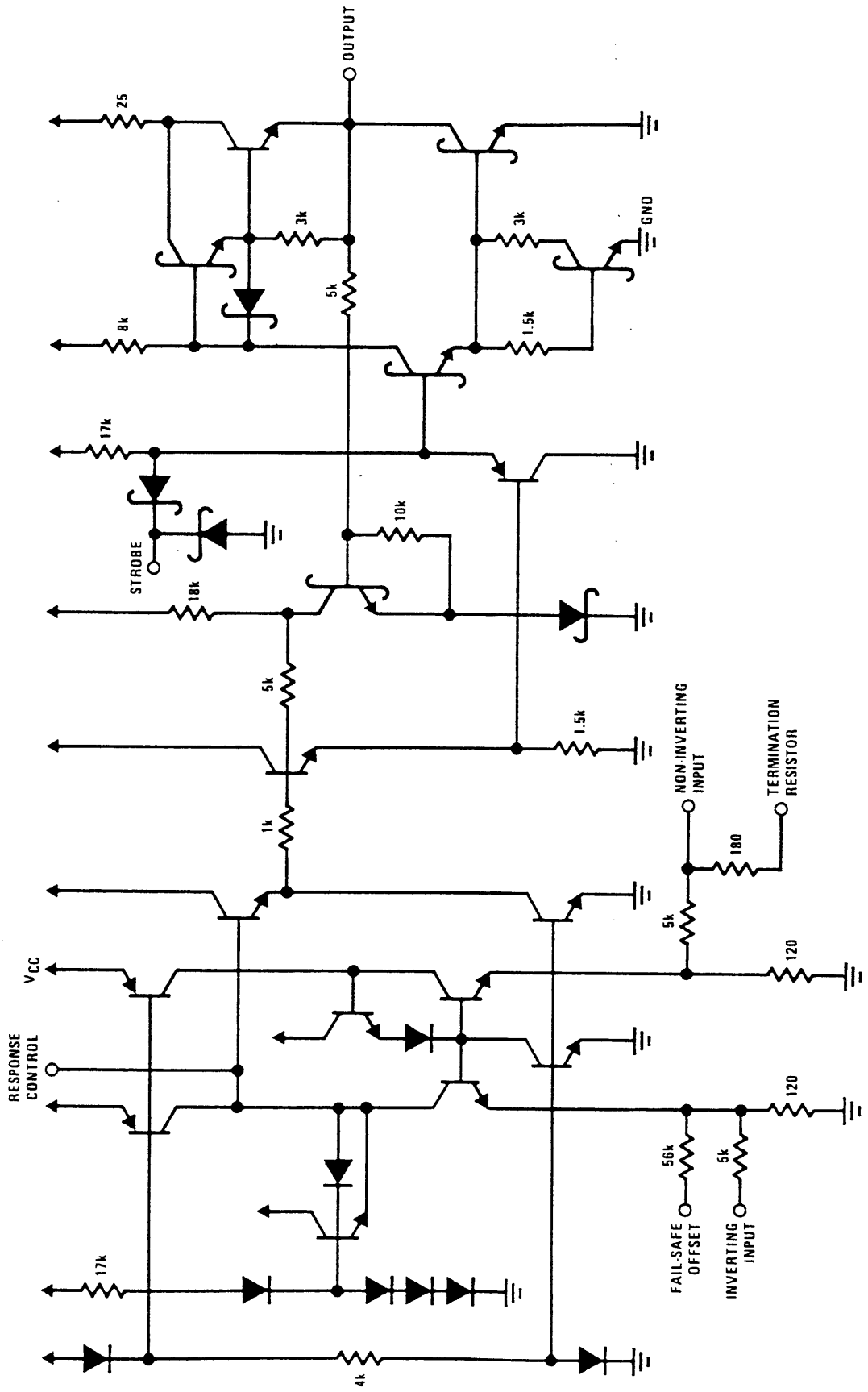
In a communications system, only the control signals are required to detect input fault conditions. Advantages of a balanced data transmission system over an unbalanced transmission system are:

1. High noise immunity
2. High data ratio
3. Long line lengths

## Truth Table (For Balanced Fail-Safe)

| Input | Strobe | A-Out | B-Out | C-Out | D-Out |
|---|---|---|---|---|---|
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 |
| X | 1 | 0 | 0 | X | 1 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| X | 0 | 1 | 1 | 0 | 0 |

## Schematic Diagram



# 16 Lead (0.150" Wide) Molded Small Outline Package, JEDEC
# NS Package Number M16A

All dimensions are in inches (millimeters)